ple, as shown in FIG. **1A**. The capacitor trench **2** has a diameter of 0.3 to 2 μm and a depth of 0.5 to 6 μm, for example. Next, the surface of the semiconductor substrate **1** is subjected to thermal-oxidization thereby forming an insulating oxide film thereon at a thickness of **10** to several tens of nm. Next, a semiconductor film **3** is deposited on the entire surface of the silicon substrate **1** by a CVD process, for example. The material of the semiconductor film **3** is poly-silicon, for example, and its thickness is about 10 to 100 nm, for example.

Thereafter, an oxidation-resistant film **4** is formed on the entire surface of the silicon substrate **1** by the CVD process, for example, as shown in FIG. **1B**. The material of this oxidation-resistant film **4** is silicon nitride, for example. A resist film **20** is then coated on the entire surface of the oxidation-resistant film **4** (FIG. **1C**). Only a portion of the resist film **20** corresponding to a part of the surface of the semiconductor substrate **1** disposed between the trenches is etched by photolithography to form a mask **22** of the resist film (FIG. **1D**). The portion of the oxidation-resistant film **4** not covered by the mask **22** is removed by dry etching, and then the mask **22** of the resist film is removed (FIG. **1E**). Next, the portion **24** of the semiconductor film **3** is subjected to thermal oxidization using the oxidation-resistant film **4** as a mask, thereby forming an element isolation film **5** (FIG. **1F**).

The conventional element isolation insulating film **102** is formed, as shown in FIGS. **3A** and **3B**, to extend partially inside the semiconductor substrate **101**. On the other hand, the element isolation insulating film **5** is formed by thermal-oxidization of the semiconductor film **3** so that the element isolation insulating film **5** projects by expansion upward relative to a level of the surface of the semiconductor substrate **1** and extends at each of both edges thereof downward into the adjacent trench because the thermal oxidization is blocked by the edge of the oxidation-resistant film **4** and advances downward along the inner wall of the trench.

Next, as shown in FIG. **1G**, the oxidation-resistant film **4** is removed by etching, and the remaining portion **6** of the semiconductor film **3** is patterned to form a first capacitor electrode **7**.

Thereafter, a capacitor insulating film **8**, a second capacitor electrode **9**, a gate insulating film **10**, a gate electrode **11** and diffusion layers **12** serving as the drain and source regions of a transistor are successively formed. In this way, a charge storage capacitor comprising the first capacitor electrode **7**, the capacitor insulating film **8** and the second capacitor electrode **9**, and a transistor comprising the gate electrode **11**, the gate insulating film **10** and the diffusion layers **12** serving as the source and drain regions is formed.

Thereafter, an inter-layer insulating film, a bit contact, a bit wire, an inter-layer insulating film, a backing wiring of the gate electrode and a passivation film (not shown) are successively formed by a known process, and a semiconductor memory device is completed.

According to the first embodiment of the present invention described above, the element isolation film **5** and the first capacitor electrode **7** are formed of the same semiconductor film **3** by one step. For this reason, the fabrication process can be simplified in comparison with the prior art process. A margin for a position error in alignment of the mask with the capacitor trench **2** for formation of the element isolation insulating film **5** and a margin for deviations in the fabrication process can be reduced, and the bird's beaks of the element isolation insulating film **5** can be reduced because it is restricted by the trenches. Accordingly, the memory cells in the semiconductor memory device can be integrated at a higher density.

Next, the second embodiment of the present invention will be explained with reference to FIGS. **2A** to **2D**. The steps of the first embodiment shown in FIGS. **1A** to **1C** are carried out similarly in this second embodiment. FIG. **2A** shows the step corresponding to the step shown in FIG. **1D**. In the second embodiment, the portion of the photoresist **20** to be removed is greater than that in the first embodiment, and a mask **22'** is formed by removing the portion having a greater width than the width between the two trenches **2**. At this time, the removed open portion of the photoresist is greater than the width between the trenches, but it does not reach a large depth of the trenches but remains at shallow portions. Accordingly, no serious problem exists even when accuracy of alignment of the mask **22'** is low. Next, the portion of the oxidation-resistant film **4** not covered by the mask **22'** is removed by dry etching so as to expose the portion **24'** of the semiconductor film (FIG. **2B**).

The photoresist is then removed (FIG. **2C**), and the portion **24'** of the semiconductor film **3** is subjected to thermal oxidization by using the oxidation-resistant film **4** as a mask to form the element isolation insulating film **5'** (FIG. **2D**). The subsequent steps are the same as those of the first embodiment.

I claim:

1. A method of manufacturing a semiconductor memory device including at least one memory cell having a transistor and a capacitor, said method comprising the steps of:

forming at least one trench in a surface of a semiconductor substrate;

forming a semiconductor film covering the surface of said semiconductor substrate and an inner wall of said trench;

forming an oxidation-resistant film to cover said semiconductor film, said oxidation-resistant film having an opening formed at its area adjacent to said trench;

oxidizing a part of said semiconductor film, which is exposed at said opening of said oxidation-resistant film, thereby forming an element isolation insulating film; and

wherein said opening extends to a part of said inner wall of said trench.

2. A method of manufacturing a semiconductor memory device according to claim **1**, wherein two trenches are formed in the surface of said semiconductor substrate, and said element isolation insulating film is disposed between said two trenches.

3. A method of manufacturing a semiconductor memory device according to claim **2**, wherein said opening is formed at its area disposed between said two trenches.

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